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EXAMINER	
HSU, JONI	
ART UNIT	**PAPER NUMBER**
2671	

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,144	ESTROP, STEPHEN J.	
	Examiner	Art Unit	
	Joni Hsu	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-13 and 15-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-13 and 15-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/2/05, 1/18/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statements (IDS) submitted on May 2, 2005 and January 18, 2005 were filed after the mailing date of the application on October 27, 2003. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Amendment

2. In light of Applicant's amendments to Claim 25, the rejection under 35 U.S.C. 112, second paragraph has been withdrawn.

3. Applicant's arguments with respect to claims 1-3, 5-13, and 15-30 have been considered but are moot in view of the new ground(s) of rejection.

4. Applicant's arguments, see pages 14-21, filed June 16, 2005, with respect to the rejection(s) of claim(s) 1-3, 5-13, and 15-27 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Uehara (US006611269B1).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1-3, 6, 9, 11-13, 16, 19, and 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salmonsen (US 20040054689A1) in view of Uehara (US006611269B1).

8. With regard to Claim 1, Salmonsen describes a method for processing video data, comprising receiving a principal video stream from a source [0104]; receiving a video sub-stream containing supplemental information associated with the principal video stream [0137]; performing an operation on the principal video stream [0104] and

combining the principal video stream with the video sub-stream to produce processed data; and outputting the processed data [0181].

However, Salmonsen does not teach that the performing and the combining are performed in a single stage operation, wherein the single stage operation requires only a single read transaction to perform the single stage operation. However, Uehara describes that arithmetic unit A (1062, Figure 1) performs an operation on the principal video stream (implements video up/down scaling processes) (Col. 4, lines 20-28; Col. 8, lines 36-37, 49-56) and arithmetic unit B (1063) combines the principal video stream with the video sub-stream to produce processed data (blending process with the on-screen display) (Col. 4, lines 20-28; Col. 8, lines 39-40, 56-61). The performing (1062) and the combining (1063) are performed in parallel (Col. 5, lines 62-67), and therefore are performed in a single stage operation, wherein the single stage operation requires only a single read transaction to perform the single stage operation (Col. 8, lines 12-22).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Salmonsen so that the performing and the combining are performed in a single stage operation, wherein the single stage operation requires only a single read transaction to perform the single stage operation as suggested by Uehara. Performing the performing and the combining in a single stage operation or in parallel allows the two processes to operate simultaneously to speed processing. The advantages of parallel processing are well-known in the art and can be found in many publications, such as the definitions of parallel processing found by Google.

9. With regard to Claim 2, Salmonsen describes that the performing of the operation comprises de-interlacing the principal video stream [0104].

10. With regard to Claim 3, Salmonsen describes that the performing of the operation comprises resizing the principal video stream [0104].

11. With regard to Claim 6, Salmonsen describes a step of forwarding instructions to a graphics processing module, the instructions informing the graphics processing module how to execute the performing and the combining (Figure 2) [0033, 0104, 0181].

12. With regard to Claim 9, Salmonsen describes that the video sub-stream includes close captioned information [0137, 0181].

13. With regard to Claim 11, Salmonsen describes an apparatus for processing video data, comprising a renderer module (514, Figure 5) [0098]; a data processing module (214, Figure 2); and an interface module (210) that couples the renderer module to the data processing module [0033], wherein the renderer module includes logic configured to generate and provide instructions to the data processing module to execute at least the following functions: a) performing an operation on a received principal video stream [0104]; and b) combining the received principal video stream with a video sub-stream [0181].

However, Salmonsen does not teach that the performing and the combining are performed in a single stage operation, wherein the single stage operation requires only a

single read transaction to perform the single stage operation. However, Uehara describes that arithmetic unit A (1062, Figure 1) performs an operation on the principal video stream (implements video up/down scaling processes) (Col. 4, lines 20-28; Col. 8, lines 36-37, 49-56) and arithmetic unit B (1063) combines the principal video stream with the video sub-stream to produce processed data (blending process with the on-screen display) (Col. 4, lines 20-28; Col. 8, lines 39-40, 56-61). The performing (1062) and the combining (1063) are performed in parallel (Col. 5, lines 62-67), and therefore are performed in a single stage operation, wherein the single stage operation requires only a single read transaction to perform the single stage operation (Col. 8, lines 12-22), as discussed in the rejection for Claim 1.

14. With regard to Claim 12, Claim 12 is similar in scope to Claim 2, and therefore is rejected under the same rationale.

15. With regard to Claim 13, Claim 13 is similar in scope to Claim 3, and therefore is rejected under the same rationale.

16. With regard to Claim 16, Claim 16 is similar in scope to Claim 6, and therefore is rejected under the same rationale.

17. With regard to Claim 19, Claim 19 is similar in scope to Claim 9, and therefore is rejected under the same rationale.

18. With regard to Claim 26, Claim 26 is similar in scope to Claim 1, and therefore is rejected under the same rationale.

19. With regard to Claim 27, Claim 27 is similar in scope to Claim 1, and therefore is rejected under the same rationale.

20. With regard to Claim 28, Salmonsen describes a method for processing video data, comprising receiving a principal video stream from a source [0104]; receiving a video sub-stream containing supplemental information associated with the principal video stream [0137]; performing an operation on the principal video stream [0104] and combining the principal video stream with the video sub-stream to produce processed data; and outputting the processed data [0181].

However, Salmonsen does not teach that the performing and the combining are performed in a single stage operation, wherein the single stage operation involves reading first input data associated with the received principal video stream in parallel with second input data associated with the received video sub-stream data. However, Uehara describes that the performing (implementing video up/down scaling processes, 1062, Figure 1; Col. 4, lines 20-28; Col. 8, lines 36-37, 49-56) and the combining (blending process with the on-screen display, 1063; Col. 4, lines 20-28; Col. 8, lines 39-40, 56-61) are performed in a single stage operation, wherein the single stage operation involves reading first input data associated with the received principal video stream in parallel with second input data associated with the received video sub-stream data (Col. 5, lines 62-67). This would be obvious for the same reasons given in the rejection for Claim 1.

21. With regard to Claim 29, Salmonsen does not teach that the single stage operation includes only one read transaction. However, Uehara describes that the performing (implementing video up/down scaling processes, 1062, Figure 1; Col. 4, lines 20-28; Col. 8, lines 36-37, 49-56) and the combining (blending process with the on-screen display, 1063; Col. 4, lines 20-28; Col. 8, lines 39-40, 56-61) are performed in parallel (Col. 5, lines 62-67), meaning that they operate at the same time, and therefore the single stage operation inherently includes only one read transaction (Col. 8, lines 13-22). This would be obvious for the same reasons given in the rejection for Claim 1.

22. With regard to Claim 30, Salmonsen does not teach that the single stage operation includes only one write transaction. However, Uehara describes that the performing (implementing video up/down scaling processes, 1062, Figure 1; Col. 4, lines 20-28; Col. 8, lines 36-37, 49-56) and the combining (blending process with the on-screen display, 1063; Col. 4, lines 20-28; Col. 8, lines 39-40, 56-61) are performed in parallel (Col. 5, lines 62-67), meaning that they operate at the same time, and therefore the single stage operation inherently includes only one write transaction. This would be obvious for the same reasons given in the rejection for Claim 1.

23. Claims 5, 7, 8, 15, 17, 18, 21, 22, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salmonsen (US 20040054689A1) and Uehara (US006611269B1) in view of Herrara (US006208350B1).

24. With regard to Claim 5, Salmonsen and Uehara are relied upon for the teachings as discussed above relative to Claim 1.

However, Salmonsen and Uehara do not teach that the performing and the combining are performed in a YUV color space. However, Herrara describes performing an operation on the principal video stream and combining the principal video stream with the video sub-stream to produce processed data (14, Figure 1; Col. 2, line 39-Col. 3, line 19), and the performing and the combining are performed in a YUV color space (Col. 2, line 51-Col. 3, line 19).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Salmonsen and Uehara so that the performing and the combining are performed in a YUV color space as suggested by Herrara. Using a YUV color space is well-known in the art and widely used. Some advantages of using a YUV color space are that they remain compatible with black and white analog television, and the signal YUV can be easily manipulated to deliberately discard some information in order to reduce bandwidth. YUV is a versatile format which can easily be combined into other legacy video formats. Combining or modulating can be accomplished easily in low-cost circuitry. The advantages of using a YUV color space can be found in many publications, such as the Wikipedia free encyclopedia.

25. With regard to Claim 7, Salmonsen and Uehara do not teach that the instructions identify a location at which to receive the principal video stream, a location at which to receive the video sub-stream, and a location at which to provide the processed data. However, Herrara describes that the instructions identify a location at which to receive

the principal video stream, a location at which to receive the video sub-stream, and a location at which to provide the processed data (Figure 7; Col. 13, lines 4-20; Col. 6, lines 12-20; Col. 15, lines 64-67).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Salmonsen and Uehara so that the instructions identify a location at which to receive the principal video stream, a location at which to receive the video sub-stream, and a location at which to provide the processed data as suggested by Herrara because Herrara suggests that the locations must be identified in the instructions so that the data will be sent to the correct destination (Figure 7; Col. 13, lines 4-20; Col. 6, lines 12-20; Col. 15, lines 64-67).

26. With regard to Claim 8, Salmonsen and Uehara do not teach that the instructions identify a rectangle of data from which to receive the principal video stream within a video stream surface, a rectangle of data from which to receive the video sub-stream within a video sub-stream surface, and a rectangle at which to output the processed data within a destination surface. However, Herrara describes that the pictures are broken into rectangles and these rectangles are mapped to the destination picture (Col. 16, lines 19-27). Therefore, the instructions must inherently identify a rectangle of data from which to receive the principal video stream within a video stream surface, a rectangle of data from which to receive the video sub-stream within a video sub-stream surface, and a rectangle at which to output the processed data within a destination surface.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Salmonsen and Uehara so that the

instructions identify a rectangle of data from which to receive the principal video stream within a video stream surface, a rectangle of data from which to receive the video sub-stream within a video sub-stream surface, and a rectangle at which to output the processed data within a destination surface as suggested by Herrara because Herrara suggests that breaking the pictures into rectangles of data makes it easier to transfer the data (Col. 15, line 64-Col. 16, line 27), and the instructions must identify the rectangles of data from which to receive the data so that the data will be sent to the correct destination.

27. With regard to Claim 15, Claim 15 is similar in scope to Claim 5, and therefore is rejected under the same rationale.

28. With regard to Claim 17, Claim 17 is similar in scope to Claim 7, and therefore is rejected under the same rationale.

29. With regard to Claim 18, Claim 18 is similar in scope to Claim 8, and therefore is rejected under the same rationale.

30. With regard to Claim 21, Salmonsen and Uehara do not teach that the data processing module comprises a graphics processing module. However, Herrara describes that the data processing module comprises a graphics processing module (92, Figure 4; Col. 10, lines 59-67).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Salmonsen and Uehara so that the data processing module comprises a graphics processing module as suggested by Herrara. Graphics processing units (GPU) are well-known in the art and are widely used. GPUs have the advantage of offloading computationally intensive transfer and lighting calculations from the CPU to the GPU, allowing faster graphics processing speeds. This means all scenes increase in detail and complexity without sacrificing performance. The advantages of GPUs can be found in many publications, such as Nvidia's website.

31. With regard to Claim 22, Salmonsen and Uehara do not teach that the graphics processing module is configured to execute video processing tasks using a graphics pipeline. However, Herrara describes that the graphics processing module (92, Figure 4) is configured to execute video processing tasks using a graphics pipeline (200, Figure 5; Col. 11, lines 18-36).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Salmonsen and Uehara so that the graphics processing module is configured to execute video processing tasks using a graphics pipeline as suggested by Herrara. Graphics pipelines are well-known in the art and are commonly implemented in graphics hardware to get interactive speeds. Graphics pipelines are discussed in many publications, such as Mann's website.

32. With regard to Claim 25, Salmonsen describes an apparatus for processing video data, comprising a memory (216, Figure 2); a computer processing module for

controlling the apparatus, the computer processing module being coupled to the memory [0042]; a renderer module (514, Figure 5) [0098]; a data processing module (214, Figure 2) coupled to the same memory as the computer processing module; and an interface module (210) that couples the renderer module to the data processing module [0033], wherein the renderer module includes logic configured to generate and provide instructions to the data processing module to execute at least the following functions: a) performing an operation on a received principal video stream [0104]; and b) combining the received principal video stream with a video sub-stream [0181], wherein the data processing module includes logic configured to receive the instructions provided by the renderer module (*content from a content source 110 can be selected through the controller 114 based on the rendering capabilities of the sink 112*, [0030]), and in response thereto, execute the performing and the combining (*executing various processes, methods, or programs*, [0033]).

However, Salmonsen does not teach that the performing and the combining are performed in a single stage operation, wherein the single stage operation requires only a single read transaction to perform the single stage operation. However, Uehara describes that arithmetic unit A (1062, Figure 1) performs an operation on the principal video stream (implements video up/down scaling processes) (Col. 4, lines 20-28; Col. 8, lines 36-37, 49-56) and arithmetic unit B (1063) combines the principal video stream with the video sub-stream to produce processed data (blending process with the on-screen display) (Col. 4, lines 20-28; Col. 8, lines 39-40, 56-61). The performing (1062) and the combining (1063) are performed in parallel (Col. 5, lines 62-67), and therefore are performed in a single stage operation, wherein the single stage operation requires only a

single read transaction to perform the single stage operation (Col. 8, lines 12-22), as discussed in the rejection for Claim 1.

However, Salmonsen and Uehara do not teach that the data processing module comprises a graphics processing module. However, Herrara describes that the data processing module comprises a graphics processing module (92, Figure 4; Col. 10, lines 59-67), as discussed in the rejection for Claim 21.

33. Claims 10 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salmonsen (US 20040054689A1) and Uehara (US006611269B1) in view of MacInnis (US006573905B1).

34. With regard to Claim 10, Salmonsen and Uehara are relied upon for the teachings as discussed above relative to Claim 1.

However, Salmonsen and Uehara do not teach that the performing and the combining are performed on an apparatus that uses a Uniform Memory Architecture (UMA) design. However, MacInnis describes performing an operation on the principal video stream (Col. 63, lines 40-51) and combining the principal video stream with the video sub-stream, which includes close captioned information (Col. 83, lines 1-5), to produce processed data in a YUV color space (Col. 5, lines 64-67; Col. 7, lines 3-10), and outputting the processed data. MacInnis also describes that the performing and the combining are performed on an apparatus that uses a Uniform Memory Architecture (UMA) design (Col. 64, lines 14-27).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Salmonsen and Uehara so that the performing and the combining are performed on an apparatus that uses a Uniform Memory Architecture (UMA) design as suggested by MacInnis because MacInnis suggests the advantage of facilitating substantial cost savings at the system level by allowing the CPU and other functions to utilize this memory at the same time that the memory is being used for graphics functions and display (Col. 64, lines 21-27).

35. With regard to Claim 20, Claim 20 is similar in scope to Claim 10, and therefore is rejected under the same rationale.

36. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salmonsen (US 20040054689A1) and Uehara (US006611269B1) in view of Heirich (US006753878B1).

37. With regard to Claim 23, Salmonsen and Uehara are relied upon for the teachings as discussed above relative to Claim 11. Uehara describes that the data processing module includes multiple processing units, wherein a first processing unit (1062, Figure 1) is allocated to a component of the received video stream (implements video up/down scaling processes) (Col. 4, lines 20-28; Col. 8, lines 36-37), and a second processing unit (1063) is allocated to the received video sub-stream (blending process with the on-screen display) (Col. 4, lines 20-28; Col. 8, lines 39-40), as discussed in the rejection for Claim 1.

However, Salmonsen and Uehara do not teach that these processing units include texturing operations. However, Heirich describes that the data processing module (image generator 12, Figure 1) includes multiple processing units (22; *image generator comprises a plurality of rendering engines 22*, Col. 5, lines 31-33) that include texturing operations (*A graphics pipeline comprises the geometry stage, the rendering stage, and the composition stage. In a rendering engine with a graphics pipeline, all of these stages are implemented*, Col. 1, lines 64-67; *in the geometry stage...the surface is bound to textures*, Col. 2, lines 1-15) and operate in parallel (*image generator 12 is parallelized, parallel rendering threads*, Col. 7, lines 33-43).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Salmonsen and Uehara so that the processing units include texturing operations as suggested by Heirich. Texturing is a method of adding realism to a computer-generated graphic. A texture is added to a simpler shape, and this reduces the amount of computing needed to create shapes and textures in the scene. The trend has recently been towards larger and more varied texture images, together with increasingly sophisticated ways to combine multiple textures for different aspects of the same object, and therefore texturing is needed. Texturing is well-known in the art, widely used, and can be found in many publications, such as the Wikipeidia Encyclopedia.

38. With regard to Claim 24, Salmonsen does not teach that the data processing module is configured to execute the performing and the combining in a single stage by processing video data obtained from the first and second texturing unit substantially in

parallel. However, Uehara describes that the data processing module is configured to execute the performing (implementing video up/down scaling processes, 1062, Figure 1; Col. 4, lines 20-28; Col. 8, lines 36-37, 49-56) and the combining (blending process with the on-screen display, 1063; Col. 4, lines 20-28; Col. 8, lines 39-40, 56-61) in a single stage by processing video data obtained from the first and second processing unit substantially in parallel (Col. 5, lines 62-67). This would be obvious for the same reasons given in the rejection for Claim 1.

However, Salmonsen and Uehara do not teach that these processing units include texturing operations. However, Heirich describes that the data processing module (image generator 12, Figure 1) includes multiple processing units (22; *image generator comprises a plurality of rendering engines 22*, Col. 5, lines 31-33) that include texturing operations (*A graphics pipeline comprises the geometry stage, the rendering stage, and the composition stage. In a rendering engine with a graphics pipeline, all of these stages are implemented*, Col. 1, lines 64-67; *in the geometry stage...the surface is bound to textures*, Col. 2, lines 1-15) and operate in parallel (*image generator 12 is parallelized, parallel rendering threads*, Col. 7, lines 33-43), as discussed in the rejection for Claim 23.

Prior Art of Record

"Parallel Processing," available at http://www.google.com/search?hl=en&lr=&oi=defmore&q=define:parallel+processing.

"YUV," available at http://en.wikipedia.org/wiki/YUV.

"GPU: Changes Everything," available at http://www.nvidia.com/object/gpu.html.

Stephen Mann, "The Graphics Rendering Pipeline," 1997, available at http://medialab.di.unipi.it/web/IUM/Waterloo/node7.html.

"Texturing mapping," available at http://en.wikipedia.org/wiki/Texture_mapping.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

Kee M. Tung
Primary Examiner